DR. BABASAHEB AMBEDKAR MARATHWADA UNIVERSITY

CIRCULAR NO. ACAD/NP/M.E./Syllabi/189/2013

It is hereby informed to all concerned that, on recommendations of the Faculty of Engineering and Technology, the Hon'ble Vice-Chancellor has accepted the following **"Revised Syllabi with Cumulative Grade Point Average [CGPA]"** under the Faculty of Engineering & Technology on behalf of the **Academic Council Under Section-14(7) of the Maharashtra Universities Act, 1994** as appended herewith :-

Sr. No.	Revised Syllabi
[1]	Revised Syllabus of M.E. [Computer Networking Engg.],
[2]	Revised Syllabus of M.E. [Structural Engineering],
[3]	Revised Syllabus of M.E. [Water Resources Engineering],
[4]	Revised Syllabus of M.E. [Environmental Engineering],
[5]	Revised Syllabus of M.E. [Software Engineering],
[6]	Revised Syllabus of M.E. [Computer Science],
[7]	Revised Syllabus of M.E. [Control System Engineering],
[8]	Revised Syllabus of M.E. [Heat Power],
[9]	Revised Syllabus of M.E. [Manufacturing Engineering],
[10]	Revised Syllabus of M.E. [Electronics],
[11]	Revised Syllabus of M.E. [Electronics & Telecommunication],
[12]	Revised Syllabus of M.E. [Embedded System],
[13]	Revised Syllabus of M.E. [Communication Engineering],
[14]	Revised Syllabus of M.E. [Digital Communication],
[15]	Revised Syllabus of M.E. [Biotechnology],
[16]	Revised Syllabus of M.E. [CAD/CAM],
[17]	Revised Syllabus of M.E. [Thermal],
[18]	Revised Syllabus of M.E. [Design Engineering],

This is effective from the Academic Year 2013-2014 and onwards.

All concerned are requested to note the contents of this circular and bring the notice to the students, teachers and staff for their information and necessary action.

University Campus,
Aurangabad-431 004.
REF.NO. ACAD/ NP/ M.E./
SYLLABI / 2013/14092-100
V.C.14[7] A-08.
Date:- 15-06-2013.

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Director,
Board of College and
University Development.

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Copy forwarded with compliments to :-

1] The Principals, affiliated concerned Colleges,
Dr. Babasaheb Ambedkar Marathwada University.

2] The Director, University Network & Information Centre, UNIC, with **a request to upload the above all syllabi on University Website [www.bamu.net].**

Copy to :-

1] The Controller of Examinations,
2] The Superintendent, [Engineering Unit],
3] The Programmer [Computer Unit-1] Examinations,
4] The Programmer [Computer Unit-2] Examinations,
5] The Superintendent, [Eligibility Unit] ,
6] The Director, [E-Suvidha Kendra], in-front of Registrar's Quarter,
Dr. Babasaheb Ambedkar Marathwada University,
7] The Record Keeper,
Dr. Babasaheb Ambedkar Marathwada University.

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S/160613/-*

DR. BABASAHEB AMBEDKAR MARATHWADA UNIVERSITY, AURANGABAD.

Revised Syllabus of

M.E. (EMBEDDED SYSTEM)

[Effective from -2013 – 2014]

Dr. Babasaheb Ambedkar Marathwada University Aurangabad.

Faculty of Engineering & Technology

Rules and Regulations for M.E. & M.Tech. Courses

➢ **What is a credit system**

A credit system is a systematic way of describing an educational program by attaching credits to its components. The definition of credits in higher education systems may be based on different parameters, such as student workload, learning outcomes and contact hours.

➢ **Advantages of the Credit System**

- Represents a much-required shift in focus from teacher-centric to learner-centric education since the work load estimated is based on the investment of time in learning, not in teaching.
- Helps to record course work and to document learner work load realistically since all activities are taken into account-not only the time learners spend in lectures or seminars but also the time they need for individual learning and the preparation of examinations etc.
- Segments learning experience into calibrated units, which can be accumulated in order to gain and academic award.
- Helps self-paced learning. Learners may undertake as many credits as they can cope with without having to repeat all the courses in a given semester if they fail in one or more courses. Alternatively, they can choose other courses and continue their studies.

➢ **What is Grading?**

The word Grade derived from the Latin word gradus, meaning, step. Grading, in the educational context is a method of reporting the result of a learner's performance subsequent to his evaluation. It involves a set of alphabets which are clearly defined and designated and uniformly understood by all the stake holders. A properly introduced grading system not only provides for a comparison of the learner's performance but it

also indicate the quality of performance with respect to the amount of efforts put in and the amount of knowledge acquired at the end of the courses by the learners.

- **CURRICULUM:**

1.1 Curriculum:

Every program with specialization has a prescribed course structure which in general terms is known as Curriculum. It prescribes course to be studied in each semester; the relevant information containing course structure along with detail syllabus for each course of each program is updated periodically and is uploaded on the website.

1.2 Semesters:

The Faculty of Engineering & Technology implements a credit based curriculum and grade based evolution system for P.G. program is of four semesters. The academic courses are delivered in the first two semesters. Dissertation work is carried out by a student in the third and fourth semester. The first semester begins in the last week of July ends by the last week of November while the second semester begins in the first week of January and ends by the second week of May. Total duration for each semester is generally of 20 weeks including the period of examination, evaluation and grade declaration.

1.3 Course Credit:

Education is organized around the semester-based credit system of study. The prominent features of the credit system are a process of continuous evaluation of a student's performance/progress and flexibility to allow a student to progress at an optimum pace suited to his/her ability or convenience, subject to fulfilling minimum requirements for continuation.

A student's performance/progress is measured by the number of credits that he/she has earned, i.e. completed satisfactorily. Based on the course credits and grades obtained by the student, grade point average is calculated. A minimum grade point average is required to be maintained for satisfactory progress and continuation in the program. Also a minimum number of earned credits and a minimum grade point average should be acquired in order to qualify for the degree. All programmers are defined by the total credit requirement and a pattern of credit distribution over courses of different categories.

1.4 Course credits assignment

Each courses, except a few special courses, has a certain number of credits assigned to it depending upon its lecture, tutorial and laboratory contact hours in a week. This weightage is also indicative of the academic expectation that includes in-class contact and self-study outside of class hours.

Lectures and Tutorials: One lecture or tutorial hour per week per semester is assigned one credit.

Practical/Laboratory: One laboratory hour per week per semester is assigned one credit.

Example: Course: XYZ Engg: 4 credits (3-1-2)

The credits indicated for this course are computed as follows:

3 hours/week lectures = 3 credits

1 hours/week tutorial = 1 credit

2 hours/week practical = 2 x 0.5 = 1 credit

2 hours/week seminar = 2 x 0.5 = 1 credit

Dissertation seminar = 2 x 1= 2 credit

(3-1-2) 3 credit course = (3 h Lectures + 1 h Tutorial + 2 h Practical) per week

= 6 Contact hours per week

1.5 Earning Credits

At the end of every course, a letter grade is awarded in each course for which a student had registered. On obtaining a pass grade, the student accumulates the course credits as earned credits. A student's performance is measured by the number of credits that he/she has earned and by the weighted grade point average.

The credit system enables continuous evaluation of a student's performance, and allows the students to progress at an optimum pace suited to individual ability and convenience, subject to fulfilling minimum requirement for continuation.

1.6 Evaluation System

1. Semester Grade Point Average (SGPA) =

   SUM (course credits in passed courses X earned grade points)

   SUM (Course credits in registered courses)

2. Cumulative Grade Point Average (CGPA) =

   SUM (course credits in passed courses X earned grade points) of all Semester
   ---
   SUM (Course credits in registered courses) of all Semester

3. At the end of M.E & M. Tech Program, student will be placed in any one of the divisions as detailed below.(According to AICTE Handbooks)

   I[st] Division with distinction : CGPA ≥ 8.25 and above

   I[st] Division : CGPA ≥ 6.75 and < 8.25

   II[nd] Division : CGPA ≥ 6.75 and < 6.25

As per AICTE Handbook (2013-14), new gradation suggested as follows,

Table 1

Grade Point	Equivalent Range
6.25	55%
6.75	60%
7.25	65%
7.75	70%
8.25	75%

Conversion of CGPA to percentage marks for CGPA ≥ 5.0 can be obtained using equations.

Percentage marks = (CGPA X10) – 7.5

An example of these calculations is given below:

Typically one example for academic performance calculations of semester -I

Table 2

Course No. (1)	Course Credit (2)	Grade Awards (3)	Earned Credit (4)	Grade Points (5)	Points Secured (6)=(4) x (5)
Subject 1	4	B	4	6	24
Subject 2	4	C	4	5	20
Subject 3	4	O	4	10	40
Subject 4	4	A+	4	8	32
Subject 5	4	C	4	5	20
Seminar	2	A++	2	9	18
Total	22		22	38	134

1. Semester Grade Point Average (SGPA) = $\frac{(134)}{(22)} = 6.09$

2. Cumulative Grade Point Average (CGPA) =
   Cumulative points earned in all passed courses = 134 (past semester) + 134 (this sem.) = 268

   Cumulative earned credits = 22 (past semesters) +22 (this sem) = 44

   $\frac{\sum (134 + 134)}{\sum (22 + 22)} = 6.09$

System Evaluation Table

Table 3

Grade	Grade Points	Marks Obtained (%)			Description Performance
		Regular Semester	Re-Examination	Summer Semester Examination/Re-appear	
O	10	91-100	--	--	Outstanding
A++	09	86-90	91-100	91-100	Excellent
A+	08	76-85	86-90	81-90	Very Good
A	07	66-75	76-85	71-80	Good
B	06	56-65	66-75	61-70	Fair
C	05	46-55	56-65	51-60	Average
D	04	40-45	40-55	40-50	Poor
F	00	Below 40	Below 40	Below 40	Fail
EE					Incomplete
WW					Withdrawal
XX	--	--	--	--	Detained
ABSENT	--	--	--	--	Absent
PP	--	--	--	--	Passed (Audit Course)
NP	--	--	--	--	Not Passed (Audit Course)

Grade Awards:

i) A ten point rating scale shall be used for the evaluation of the performance of the student to provide letter grade for each course and overall grade for the Master's Programme. Grade points are based on the total number of marks obtained by him/her in all the heads of examination of the course. These grade points and their equivalent range of marks are shown separately in Table-4.

Table 4: Ten point grades and grade description

Sr.No.	Equivalent Percentage	Grade Points	Grade	Grade Description
1	90.00 – 100	10	O	Outstanding
2	80.00 – 89.99	9	A++	Excellent
3	70.00 – 79.99	8	A+	Exceptional
4	60.00 – 69.99	7	A	Very Good
5	55.00 – 59.99	6	B+	Good
6	50.00 – 54.99	55	B	Fair
7	45.00 – 49.99	5	C+	Average
8	40.01 – 44.99	4.5	C	Below Average
9	40	4.00	D	Pass
10	<40	0.00	F	Fail

ii) Non appearance in any examination/assessment shall be treated as the student have secured zero mark in that subject examination/assessment.

iii) Minimum D grade (4.00 grade points) shall be the limit to clear/pass the course/subject. A student with F grade will be considered as 'failed' in the concerned course and he/she has to clear the course by reappearing in the next successive semester examinations. There will be no revaluation or recounting under this system.

iv) Every student shall be awarded Grade points out of maximum 10 points in each subject (based on 10 Point Scale). Based on the Grade points obtained in each subject, Semester Grade Point Average (SGPA) and then Cumulative Grade Point Average (CGPA) shall be computed. Results will be announced at the end of each semester and cumulative Grade card with CGPA will be given on completion of the course.

Proposed Coding System of M.E/M.Tech Subjects

Six Digit Code for a subject (PG Course)

	Digits→	1 2 3	4	5 6
Sr. No.	**Branch** ↓	**Branch code**	**Year**	**Subject**
1	Electronics	MEX	PG I year – 6	**Semester –I/III**
2	Communication Engineering	MEC	PG II Year - 7	1-20 Theory
3	Electronics & Telecom.	MET		21-30 Practical
4	Digital Communications	MDC		31 Dissertation-I
5	Embedded System	MES		41-49 Electives
6	Structure Engineering	MSE		**Semester –II/IV**
7	Environmental Engineering	MEV		51-70 Theory
8	Water Resource Engineering	MWR		71-80 Practical
9	Computer Engineering	MCE		81 Dissertation-II
10	Computer Network	MCN		91-99 Electives
11	Software Engineering	MSW		
12	Mechanical Engineering	MME		
13	Thermal Engineering	MTE		
14	CAD/CAM	MCC		
15	Manufacturing	MMF		
16	Heat Power	MHP		
17	Machine Design	MMD		
18	M.Tech Mechanical	MTM		
19	CSE & IT	MCI		
20	Manufacturing Processing Engineering	MMP		

Note: - Kindly, Allot Same Code for same Electives/ subjects for different branches to avoid repetitions of Question papers/settings/assessments.

DEGREE OF MASTAR OF ENGINEERING
(Course with effective from academic year: 2013-2014)

I	1	The examination for the Degree of Master of Engineering will be held in four semesters, M.E. Semester-I, M.E. Semester-II, M.E. Semester-III, and M.E. Semester-IV in case of full time course.
II	**Rules & Eligibility**	
	1	Rule for admission to P.G. Degree course in Engineering and Technology as per rules and regulation of AICTE/DTE & Dr. Babasaheb Ambedkar Marathwada University, Aurangabad.
III	**Evaluation method**	
	1	Each theory course will be of 100 marks and be divided in to internal examination of 20 marks and semester examination of 80 marks (20+80=100 marks). Each practical course will be of 50 marks
	2	There shall be two class tests within a semester. First based on 40% syllabus taught and second based on 60% syllabus taught. The setting of question paper and assessment will be done by the concerned teacher who has taught the syllabus. Average marks obtained out of two examinations will be considered for the preparation of final sectional marks/ grade.
	3	The Question papers in theory subjects shall be set by the Examiners appointed for the purpose by the University on the recommendations of the Board of studies of the concerned PG Course.
	4	The assessment of the term work for any subject will be done by recognized post-graduate teacher.
	5	To pass the examination a candidate must obtain a minimum CGPA of 6.25 (CGPA to the scale of 10).
	6	Candidate who secures CGPA $\geq$ 6.25 and CGPA < 6.75 declared to have passed examination in second class.
	7	Candidate who secures CGPA $\geq$ 6.75 and CGPA < 8.25 declared to have passed examination in first class.
	8	Candidate who secures CGPA $\geq$ 8.25 declared to have passed examination in first class with distinction.

IV	1	In case candidate fails to get D grade in one or more heads of passing examination, he will be allowed at his option, to reappear for only those heads of passing in which he has failed or got less than D grade at subsequent examinations.
	2	The grades obtained by the candidate in any head of passing at the examination will be carried forward unless the candidates reappear for the head of passing in accordance with ref. IV (1)
	3	In case the candidate passes in all heads of passing under M.E. Semester-I, M.E. Semester-II examination and obtained a minimum CGPA of 6.25 in M.E. Semester-I, M.E. Semester-II taken together as required under ref. II(2) above, he will not be allowed to reappear for any head of passing under M.E. Semester-I, M.E. Semester-II in accordance with ref. IV(1)
	4	A candidate will not be allowed to appear for M.E. Semester-III examination unless he passes in all heads of passing under M.E. Semester-I, M.E. Semester-II examination and obtains a minimum CGPA of 6.25 in M.E. Semester-I, M.E. Semester-II taken together under reference II(2).
	5	Whenever a candidate reappears for M.E. Semester-III and M.E. Semester-IV examinations he will have to resubmit the dissertation with suitable modification and must also reappear for oral examination on it.
	6	A candidate registered for M.E. Examination must clear his examination within five years from the date of registration.
V	**Attendance Requirement**	
	1	Each semester of the course shall be treated as a separate unit for calculation of the attendance
	2	A candidate shall be considered to have satisfied the attendance requirement if he/she has attended not less 75% of the class in each subject of all the semesters (Theory, Laboratory, Semester Practical training and Dissertation work) actually conducted up to the end of the semester.
	3	A Candidate, who does not satisfy the attendance required, mentioned as above, shall not be eligible to appear for the Examination of that semester and shall be required to repeat that semester along with regular students later.
	4	The Principal of the concerned College shall display regularly, the list of such candidates who fall short of attendance, on the Notice Boards.

	5	The list of the candidates falling short of attendance shall be sent to the University at least one week prior to the commencement of theory/practical examination, whichever is earlier.
VI		The following are the syllabi in the various subjects of the examination for the Degree of Master of Engineering.

Dr Babasaheb Ambedkar Marathwada University, Aurangabad

Proposed Syllabus Structure of M.E. (Embedded System) w.e.f. Academic Year 2013-14

Semester-I

Course code	Name of the Subject	Teaching Scheme Contact hours per week				Examination scheme Marks					Duration of Theory Exam	Credit
		L	T	P	Total hrs	Theory	Class Test	Term Work	Viva voce	Total		
ME0601	Advanced Digital Signal Processing	3	1		4	80	20			100	3 Hrs	4
ME0602	Advanced Digital Communication System	3	1		4	80	20			100	3 Hrs	4
MES603	Design With Microcontroller	3	1		4	80	20			100	3 Hrs	4
MES604	VLSI Design	3	1		4	80	20			100	3 Hrs	4
MES(641-643)	Elective –I	3	1		4	80	20			100	3 Hrs	4
MES621	Embedded Lab-I			4	4			50	-	50		2
MES622	System lab-I			2	2			-	50	50		1
MES623	Seminar-I			2	2			-	50	50		1
	Total	**15**	**5**	**8**	**28**	**400**	**100**	**50**	**100**	**650**		**24**

Semester-II

Course code	Name of the Subject	Teaching Scheme Contact hours per week				Examination scheme Marks					Duration of Theory Exam	Credit
		L	T	P	Total hrs	Theory	Class Test	Term Work	Viva voce	Total		
ME0651	Advanced Optimization Techniques	3	1		4	80	20			100	3	4
ME0652	Audio Signal Processing & Coding	3	1		4	80	20			100	3	4
MES653	Embedded System Design	3	1		4	80	20			100	3	4
ME0654	Real Time Operating System	3	1		4	80	20			100	3	4
MES691-693	Elective -II	3	1		4	80	20			100	3	4
MES671	Embedded Lab-II			4	4			50	-	50		2
MES672	System Lab-II			2	2			-	50	50		1
MES673	Seminar-II			2	2			-	50	50		1
	Total	**15**	**5**	**8**	**28**	**400**	**100**	**50**	**100**	**650**		**24**

Semester III

Course code	Name of the Subject	Teaching Scheme Hrs per week			Examination scheme Marks				Credit
		L	CH	Total hrs	Theory	Term work	Viva voce	Total	
MES 731	Dissertation Phase I	--	12	12	--	50	50	100	12
	Total	--	**12**	**12**	--	**50**	**50**	**100**	**12**

Semester IV

Course code	Name of the Subject	Teaching scheme Hrs per week			Examination scheme Marks				Credit
		L	CH	Total hrs	Theory	Term work	Viva voce	Total	
MES 781	Dissertation Phase II	--	20	20	--	100	200	300	20
	Total	--	**20**	**20**	--	**100**	**200**	**300**	**20**
	Grand Total							**1700**	**80**

Elective - I
MES641 –Image & Video processing
MES642 - Artificial Intelligence
MES643 -Advanced Computer Architecture

Elective - II
MES691 -Advanced Computer Architecture
MES692 -Statistical Signal processing
MES693 -Reconfigurable Computing

L: Lecture hours per week T: Tutorial Hours per week P: Practical hours per week CH: Contact hours

Total Credits = SEM I + SEM II + SEM III + SEM IV
= 24 + 24 + 12 + 20
= 80

SEMESTER-I

ME0601 - ADVANCED DIGITAL SIGNAL PROCESSING

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(04Hrs)**

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN

Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT 2. **(08Hrs)**

DIGITAL FILTER SRTUCTURE AND DESIGN

All Pass Filters, Tunable IIR Digital Filter, IIR Tapped Cascade Lattice Structures, FIR Cascaded Lattice Structures, Parallel All Pass Realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine Cosine Generator, Computational Complexity of Digital Filter Structures, Design of IIR Filter using pade' approximation, Least Square Design Methods, Design of Computationally Efficient FIR Filters.

UNIT 3. **(08Hrs)**

MULTI RATE SIGNAL PROCESSING

Mathematical description of change of sampling rate Interpolation and Decimation , Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter implementation for sampling rate conversion- direct form FIR structures, Polyphasefilter structures, time-variant structures. Multistage implementation of multirate system.

UNIT 4. **(08Hrs)**

LINEAR ESTIMATION AND PREDICTION

Linear prediction- Innovations representation of a stationary Random process, Relationship between the filter parameters and the autocorrelation sequence, Autoregressive (AR) & moving average (MA) process,Forward and backward predictions, Solutions of the Normal equations-Levinson-Durbin algorithms. Least mean squared error criterion -Wiener filter for filtering and prediction, FIR Wiener filter and Wiener IIR filters.

UNIT 5. **(08Hrs)**

POWER SPECTRAL ESTIMATION

Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch &Blackmann&Tukey methods. Parametric Methods For Power Spectrum Estimation: Relation between auto correlation & model parameters, Yule-Waker& Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT 6. **(04Hrs)**

ADAPTIVE FILTERS

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR).

REFERENCES:

1. Monson H. Hayes, *"Statistical Digital Signal Processing and Modeling"*, John Wiley and Sons, Inc., Singapore, 2002.
2. John G. Proakis, Dimitris G. Manolakis, *"Digital Signal Processing"*, Pearson Education, 2002.
3. John G. Proakis *"Algorithms for Statistical Signal Processing"*, Pearson Education, 2002.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, *"Digital Signal Processing"* – A Practical Approach, Addison Wesley, 1993.
5. A.V. Oppenheim and Schafer, *"Discrete Time Signal Processing"*, Prentice Hall, 1989.
6. *"Texas Instruments"*, Users Guide TMS320C50.

SEMESTER-I

ME0602 - ADVANCED DIGITAL COMMUNICATION SYSTEM

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(04 Hrs)**

INTRODUCTION: Digital communication system (description of different modules of the block diagram), Complex baseband representation of signals, Gram-Schmidtorthogonalization procedure. M-ary orthogonal signals, bi-orthogonal signals, simplex signal waveform

UNIT 2. **(08 Hrs)**

MODULATION: Pulse amplitude modulation (binary and M-ary, QAM), Pulse position modulation (binary and M-ary), Carrier modulation (M-ary ASK, PSK, FSK, DPSK), Continuous phase modulation (QPSK and variants, MSK, GMSK).

UNIT 3. **(08 Hrs)**

RECEIVER IN ADDITIVE WHITE GAUSSIAN NOISE CHANNELS: COHERENT AND NO COHERENT DEMODULATION: Matched filter, Correlator demodulator, square-law, and envelope detection; Detector: Optimum rule for ML and MAP detection Performance: Bit-error-rate, symbol error rate for coherent and no coherent schemes.

UNIT 4. **(10 Hrs)**

BAND-LIMITED CHANNELS: Pulse shape design for channels with ISI: Nyquist pulse, Partial response signaling (duo binary and modifiedduobinary pulses), demodulation; Channel with distortion: Design of transmitting and receiving filters for a known channel and for time varying channel (equalization); Performance: Symbol by symbol detection and BER, symbol and sequence detection, Viterbi algorithm.

UNIT 5. **(04 Hrs)**

SYNCHRONIZATION: Different synchronization techniques (Early-Late Gate, MMSE, ML and spectral line methods).

UNIT 6. **(06 Hrs)**

COMMUNICATION OVER FADING CHANNELS: Characteristics of fading channels, Rayleigh and Ricianchannels, receiver performance-average SNR, outage probability, amount of fading and average bit/symbol error rate.

REFERENCES BOOKS:

1. J. G. Proakis and M. Salehi, Fundamentals of Communication Systems,Pearson Education, 2005.

2. S. Haykins, Communication Systems, 5th ed., John wiley, 2008.

3. M. K. Simon, S. M. Hinedi and W. C. Lindsey, Digital Communication Techniques: Signaling and detection, Prentice Hall India, N. Delhi, 1995.

4. W. Tomasi, Advanced Electronic Communication Systems, 4th Ed., Pearson Education, 1998.

SEMESTER-I

MES603– DESIGN WITH MICROCONTROLLER

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(06 Hrs)**

INTRODUCTION TO ATMEL® AVR® 32-BIT MICROCONTROLLERS: Features, Architecture, Programming Model, Data Organization, Processor States, Memory Management Unit, Memory Protection Unit

UNIT 2. **(05 Hrs)**

AVRPROGRAMMING:RISC Instruction Set, Assembly/C Language Programming

UNIT 3. **(10 Hrs)**

PIC MICROCONTROLLER : 16-bit PIC microcontroller Architecture, Memory Organization, Flash program memory, Programming Flash program memory, Erasing a program memory , Resets, Interrupt Controller ,IVT, Interrupt Control and Status Registers, Oscillator Configuration, Power-Saving features .
(PIC24FJ128GA010 as reference microcontroller)

UNIT 4. **(10Hrs)**

PIC PROGRAMMING: Instruction Set, Special Function Registers, Assembly/C Language Programming (Take **PIC24FJ128GA010 as reference microcontroller)**

UNIT 5. **(05 Hrs)**

ON CHIP PERIPHERALS AND INTERFACING: I/O Ports, Timers/Counters, The Watchdog Timer, Data Converters(ADC,DAC), RTC, Serial Communication, Interfacing of LCD, LED display, Keyboard and Flash Program Memory, Interrupts, SPI & I2C Communication Buses

UNIT 6. **(04 Hrs)**

APPLICATION DEVELOPMENT: Tools for system development such as Assembler, Compiler, In-Circuit Emulator, Simulator, Data acquisition and manipulation applications, Actuators: motors and servos applications, Sensor Interfacing, PIC System Design.

REFERENCE BOOKS:

1. Microcontrollers: From Assembly Language to C Using the PIC24 Family. By: Robert Reese; Bryan Jones; J.W.Bruce, Publisher: Course Technology PTR
2. Interfacing PIC Microcontrollers-Embedded Design By Interactive Simulation by Martin Bates, Newnes.
3. PIC Microcontroller [Paperback] Muhammad Ali Mazidi (Author), Rolin D. McKinlay (Author), Danny Causey (Author)
4. Microchip PIC Data Sheet PIC24FJ128GA010 Family Data Sheet
5. Atmel AVR@32 bit Microcontroller Data Sheet

SEMESTER-I

MES604 – VLSI DESIGN

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT1. **(04 Hrs)**

MOS INVERTER:
Introduction, MOS Inverter and its characteristics: C-V Characteristics, Nonideal I-V Effect,Dc Transfer Characteristics, Threshold voltage equations, Body effects, MOS device Design equations, Basic DC equations, Latch-up in CMOS circuits and other second order effects.

UNIT2. **(04 Hrs)**

INTRODUCTION TO CMOS CIRCUITS: CMOS Logic- Complementary CMOS inverter- DC Characteristics, Noise margin, Static load MOS Inverters, Differential Inverter, the transmission gate, Tristate Inverter, Bi-CMOS Inverters, SPICE Model; Combination logic- static and dynamic design strategies, The NAND and NOR Gates, Compound gates, Multiplexers.

UNIT3. **(08 Hrs)**

DESIGNING COMBINATIONAL LOGIC GATES IN CMOS:
Static CMOS Design, Dynamic CMOS Design,More Circuit Families: Differential Circuits, Sense amplifier, BiCMOS Circuits.

UNIT4. **(08 Hrs)**

DESIGNING SEQUENTIAL LOGIC CIRCUITS: Static latches and registers, Dynamic latches and registers, non bistable sequential circuits.

UNIT5. **(08 Hrs)**

DATAPATH SUBSYSTEMS AND: Addition, Subtraction, Parity Generator, Comparator, Counters, Shifters, Multiplication and other arithmetic operators; power and speed tradeoffs, Control FSM and Control Logic Implementation.

UNIT6. **(08 Hrs)**

ARRAY SUBSYSTEMS: Memory cells and Arrays, ROM, RAM- SRAM, DRAM, clocking disciplines; Design, power optimization, case studies in memory design.

REFERENCE BOOKS:

N. Waste and K. Eshranghian, "Principals of CMOS VLSI Design", Addison Wesley

Jan Rabaey,Anantha Chandrakasan and Borivoje Nikolic, "Digital IntegratedCircuits"

Jacob Backer, Harry W. Lie and Devid E. Boyce,"CMOS Circuit Design , Layout and Simulation" Prentice Hall.

L.Glaser and Dobberpuhi, "The Design and Analysis of VLSI Circuits", Addison Wesley

Mnnn, "Introduction to VLSI System" Addison Wesley

Dr. K.V.K.K. Prasad, Kattula Shyamala, "VLSI Design Black Book":

John P. Uyemura, "Introduction To VLSI Circuits And Systems" Wiley Pub

SEMESTER-I

MES641 – IMAGE AND VIDEO PROCESSING (EL-I)

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08 Hrs)**

IMAGE AND VIDEO ENHANCEMENT AND RESTORATION:

Basic Linear Filtering with Application to Image Enhancement ,Nonlinear Filtering for Image Analysis and Enhancement ,Morphological Filtering for Image Enhancement and Detection, Basic Methods for Image Restoration and Identification, Motion Detection and Estimation, Video Enhancement and Restoration

UNIT 2. **(08 Hrs)**

IMAGE REPRESENTATIONS AND IMAGE MODELS:
Computational Models of Early Human Vision , Multiscale Image Decompositions and Wavelets, Random Field Models, Statistical Methods for Image Segmentation, Video Segmentation

UNIT 3. **(06 Hrs)**

IMAGE COMPRESSION:
Lossless Coding,Block Truncation Coding , The JPEG Lossy Image Compression Standard, The JPEG Lossless Image Compression Standards

UNIT 4. **(06 Hrs)**

VIDEO COMPRESSION:
Basic Concepts and Techniques of Video Coding and the H.261 Standard, Object-Based Video Coding, MPEG- 1 and MPEG-2 Video Standards, Emerging MPEG Standards: MPEG-4 and MPEG-7.

UNIT 5. **(06 Hrs)**

IMAGE AND VIDEO ACQUISITION:

Image Scanning. Sampling. and Interpolation ,Video Sampling and Interpolation

UNIT 6. **(06 Hrs)**

IMAGE AND VIDEO RENDERING AND ASSESSMENT APPLICATIONS:

Image Quantization. Halfioning. and Printing ,Perceptual Criteria for Image Quality Evaluation, Fingerprint Classification and Matching, Human Face Recognition.

REFERENCE BOOKS:

1.Al Bovik:Handbook of Image & Video Processing Academic Press

2.J. W. Woods :Multidimensional Signal, Image and Video Processing and Coding, , Academic Press

3.A. M. Tekalp :Digital Video Processing, Prentice Hall

4.Y. Wang, J. Ostermann, and Y.-Q. Zhang : Video Processing and Communications, Prentice Hall, 2002

SEMESTER-I

MES642 – ARTIFICIAL INTELLIGENCE (EL-I)

Teaching Scheme:	Examination Scheme:
Lecture - 03 Hrs	Theory Paper - 80 Marks
Tutorial - 01 Hrs	Class Test - 20 Marks
	Credit:-04

UNIT 1. **(06 Hrs)**

INTRODUCTION:

Introduction to Artificial Intelligence, History of artificial intelligence, Intelligent Agents, Agents and environments, Good behavior, The nature of environments, structure of agents, Problem Solving , problem solving agents , example problems , searching for solutions, uniformed search strategies DFS,BFS.

UNIT 2. **(08 Hrs)**

SEARCHING TECHNIQUES:

Informed search and exploration , Informed search strategies , heuristic function , local search algorithms and optimistic problems, local search in continuous spaces , online search agents and unknown environments, Constraint satisfaction problems (CSP), Backtracking search and Local search for CSP, Structure of problems, Adversarial Search, Games, minimax algorithm, Optimal decisions in games, Alpha, Beta Pruning.

UNIT 3. **(06 Hrs)**

KNOWLEDGE REPRESENTATION & REASONING:

Foundations knowledge representations and reasoning, First order logic, representation revisited, Syntax and semantics for first order logic, Inference in First order logic, prepositional versus first order logic, unification and lifting, forward chaining, backward chaining, Resolution, Knowledge representation, Reasoning with defaults, Reasoning about knowledge, sample applications.

UNIT 4. **(06 Hrs)**

KNOWLEDGE ENGINEERING & PLANNING:

Ontology, Categories and objects, Actions - Simulation and events, Mental events and mental objects, Planning problem, Planning with State Space Search, Partial order planning,

Hierarchical Planning, Conditional Planning.

UNIT 5. **(08 Hrs)**

LEARNING:
Learning from observations, forms of learning, Inductive learning, Learning decision trees, Ensemble learning, Logical formulation of learning, Explanation based learning, Learning using relevant information, Statistical learning methods, Learning with complete data, Learning with hidden variable, EM algorithm, Genetic algorithm, Instance based learning, Neural networks, Perceptrons, Reinforcement learning : Passive & Active reinforcement learning, Generalization in reinforcement learning, Applications of ANN.

UNIT 6. **(06 Hrs)**

COMMUNICATION:
Communication as action, Formal grammar for a fragment of English, Syntactic analysis, Augmented grammars, Semantic interpretation, Ambiguity and disambiguation.

TEXT BOOKS:

1. S. Russel and P. Norvig, "Artificial Intelligence – A Modern Approach", Second Edition, Pearson Education, 2003.

REFERENCE BOOKS:

1. G. Luger, "Artificial Intelligence: Structures and Strategies for complex problem solving", Fourth Edition, Pearson Education, 2002

2. Patrick H. Winston, Artificial Intelligence, 3rd edition, Pearson.

SEMESTER-I

MES643 – ADVANCED COMPUTER ARCHITECTURE (EL-I)

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08 Hrs)**

INTRODUCTION TO SUBJECT: Principles of scalable performance:-Performance metrics and measures, parallel processing applications, scalability analysis and approaches.
Bus, cache and shared memory:-Back plane bus systems, Cache memory organization and shared memory organizations. Flynn's classifications.

UNIT 2. **(07 Hrs)**

PIPELINING TECHNIQUES:- Linear pipeline processors, nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design.

UNIT 3. **(07 Hrs)**

SUPER SCALAR TECHNIQUES: Super scalar and super-pipeline design
SIMD array processors: - features and organization, interconnecting networks, parallel algorithms for array processors,

UNIT 4. **(06 Hrs)**

ASSOCIATIVE ARRAY PROCESSING AND PROCESSORS: Performance enhancement of array processors. Vector processing principles and vector instructions, Vector processors

UNIT5. **(06 Hrs)**

MULTIPROCESSOR AND MULTICOMPUTER:-Structures, multiprocessor system interconnects, cache coherence and synchronization mechanisms, Three generations of multi-computers , message passing mechanisms.

UNIT 6. **(06 Hrs)**

RISC PROCESSORS: The VLIW Architecture, case studies of at least two of the architectures studied above.
Brief introduction to parallel processing models and languages

REFERENCE BOOKS:

1. Advanced Computer Architecture by Kai Wang ,TMH.
2. Computer Architecture and parallel preprocessing, by Kai Wang and F.A.Briggs. Mc Graw Hill (IE)
3. Computer Organization and Architecture by W. Stalling, MC Millan.
4. High Performance Computer Architecture H.S.Store, Addition Wesley.
5. Modern processor Design: Fundamentals of Super scalar Processors She
6. Computer Architecture And Organization An Integrated Approach By Miles Murdocca And Vincent Heuring
7. Comuter System Architecture And Organization By Dr. M.Usha And T.S. Shrikanth

SEMESTER-I

MES621 – EMBEDDED LAB-I

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Practical Hours:-04 H/Week	Term work:-50 Marks
	Credit:-02

Students are instructed to frame and perform laboratory assignment based on each of theory course. The assignment should encompass the hardware and software techniques/tools introduced in the concerned subjects and should prove to be useful for the PG program in the relevant field. Assignment should be a full-fledged system design problems with multidimensional solutions suggested.

Student shall submit a laboratory work document based on the assignment performed at the end of semester. The laboratory instructor shall guide the students in framing the assignments and defining the problems pertaining to the said subjects.

SEMESTER-I

MES622 – SYSTEM LAB-I

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Practical Hours-02 H/Week	Practical- 50 Marks
	Credit-01

Individual student will perform the work as per the following guidelines and submit the report based on result obtained and /or study performed under the guidance of respective guide (Minimum 25 pages).

The work will be assessed by two examiners out of which one will be external examiner appointed by the University and second examiner (internal) will be guide itself.

Work to be carried out by student,

1) Student should perform experimentation in any subject of the stream as assign by the respective guide, leading towards concept understanding.
2) Literature survey about the topic, research and development or thrust area subject.
3) Student should study any one of the software from given list and develop a specific software based module using C/C++/Vb/Matlab/VHDL/Microwind/LabView/PSpice/ EDA or ECAD etc.

SEMESTER-I

MES623 – SEMINAR-I

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Hours:-02 H/Week	Seminar:-50 Marks
	Credit:-01

Student should deliver seminar on the state of the art topic infront of the external examiners and internal examiners, staff and student colleagues. Prior to presentation student should carry the details of literature survey form standard references such as international journals and periodicals, recently published reference books etc. student should submit a report on same along with computer based presentation copy to the concerned examiner/guide at the end of seminar. The assessment shall be based on selection of topic its relevance to present context, report documentation and presentation skills.

SEMESTER-II

ME0651 – ADVANCED OPTIMISATION TECHNIQUES

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(02Hrs)**

INTRODUCTION: Optimal problem formulation, engineering optimization problems, optimization Algorithms.

UNIT 2. **(06Hrs)**

SINGLE VARIABLE OPTIMIZATION ALGORITHMS: Optimality criteria, bracketing methods, region elimination methods, point estimation methods, gradient base, root finding using optimization Techniques.

UNIT 3. **(08Hrs)**

MULTIVARIABLE OPTIMIZATION ALGORITHMS: Optimality criteria, unidirectional search, direct Search methods, gradient based methods, computer programs on above methods.

UNIT 4. **(08Hrs)**

CONSTRAINED OPTIMIZATION ALGORITHMS: Kuhn-Tucker conditions, transformation methods, sensitivity analysis, direct search for constrained minimization, linearised search techniques, feasible direction method, generalized reduced gradient method, gradient projection method, computer programs on above methods.

UNIT 5. **(08Hrs)**

SPECIAL OPTIMIZATION ALGORITHMS: Integer programming, Geometric programming, Genetic Algorithms, simulated annealing, global optimization, Computer programs on above methods.

UNIT 6. **(08Hrs)**

OPTIMIZATION IN OPERATIONS RESEARCH: Linear programming problem, simplex method, artificial variable techniques, dual phase method, sensitivity analysis

REFERENCE BOOKS:

1. Deb Kalyanmoy, "Optimization in Engineering Design", PHI, New Delhi.
2. Rao S.S. "Engineering Optimization", John Wiley, New Delhi.
3. Deb Kalyanmoy, "Multi-objective Algorithms using Evolutionary Algorithms", John Wiley, New Delhi.
4. Paplambros P.Y. and Wilde D.J., "Principles of Optimum Design: Modeling and Computation", Cambridge
University Press, UK
5. Chandrupatla, "Optimization in Design", PHI, New Delhi.

SEMESTER-II

ME0652 – AUDIO SIGNAL PROCESSING AND CODING

Teaching Scheme:	Examination Scheme:
Lecture - 03 Hrs	Theory Paper - 80 Marks
Tutorial - 01 Hrs	Class Test - 20 Marks
	Credit:-04

UNIT 1. **(04 Hrs)**

FUNDAMENTALS OF SPEECH Nature of Speech ,type of speech, voiced an unvoiced decision making, audio file formats, process of speech production, acoustic theory of speech production.

UNIT 2. **(04 Hrs)**

DIGITAL MODELS FOR THE SPEECH SIGNAL: Lossless tube models and Digital models for speech signals, time domain model for speech processing, time dependent processing of speech, parameter of speech: pitch &formats, fundamental frequency or pitch frequency, Parallel Processing Approach for calculation of pitch frequency, pitch period measurement using spectral domain, cepstral domain, estimation of formats.

UNIT 3. **(08 Hrs)**

SPECTRAL PARAMETER OF SPEECH: Homomorphic Processing, Cepstal analysis of speech, the auditory system as a filter bank,perceptual linear prediction, log frequency power coefficients, relative spetral perceptual linear prediction,short-time spectral analysis of speech, wavelet transformation analysis of speech.

UNIT 4. **(08 Hrs)**

SPEECH QUANTIZATION AND CODING: Uniform and non-uniform quantization and coder, companded quantizer, waveform coding of speech, comparison of different waveform coding techniques, parameter speech coding technique, mixed excitation linear prediction coder,multi-mode speech coding, transform domain coding of speech.

UNIT 5. **(08 Hrs)**

SHORT TIME FOURIER ANALYSIS: Linear filtering interpretation, filter bank summation method, overlap addition method, design of digital filter bank, implementation using FFT, spectrographic displays, pitch detection, analysis by synthesis,analysis sysnthesis system,

Homomorphic speech processing: Homomorphic system for convolution, complex spectrum, pitch detection, format estimation ,Homomorphic vocoder.

UNIT 6. **(08 Hrs)**

SPEECH SYNTHESIS AND SPEECH PROCESSING APPLICATION: A text to speech system, synthesizer technologies ,speech sysnthesis using other methods, speech transformations, emotion recognition from speech, speech recognition for ASR, statical sequence recognition for ASR, VQ-HMM- based speech recognition, word spotting/key-word spotting, speaker recognition, speech enhancement, adaptive echo cancellation, audio processing: auditory perception and psychoacoacoustis masking frequency and loudness perception, spatial perception, digital audio, audio coding, high quality, low bit rate, audio coding standard, MPEG,AC-3

TEXT BOOKS:

1. L.R.Rabiner and R.W. Schafer, "Digital processing of speech signal" Pearson Education (Asia) Pte.Ltd, 2004

2. D.O'Shaughnessy "Speech Communication: Human and Machine"Universities Press2001

3.L.R. Rabiner and B.Juang "Fundamentals of Speech Recognition"Pearson Education Pte.Ltd, 2004

4.Z.Li and M.S. Drew "Fundamentals of Multimedia" Pearson Education Pte.Ltd, 2004

5.Shaila D Apte "Speech and Audio Processing" John Wiley & Sons

REFERENCE BOOKS :

1. C Becchetti & L P Ricotti,"Speech Recognition Theory & C++ Implementation" John Wiley & Sons
2. . B Gold & N. Morga "Speech & Audio Signal Processing",John Wiley & Sons.

SEMESTER-II

MEX653 – EMBEDDED SYSTEM DESIGN

Teaching Scheme:	Examination Scheme:
Lecture - 03 Hrs	Theory Paper - 80 Marks
Tutorial - 01 Hrs	Class Test - 20 Marks
	Credit:-04

UNIT 1. **(12Hrs)**

INTRODUCTION: EMBEDDED SYSTEMS overview, Design Challenges, Processor Technology, IC Technology, Design Technology, Trade-offs, Custom Single purpose processors, RT level Custom Single purpose processor design, Optimization, General Purpose processors: pipelining, superscalar and VLIW architectures, Programmers view: Instruction set, program and data memory space, I/O, interrupts, operating system.
Development environment: design flow and tools, testing and debugging, Application specific instruction set processors (ASIPs), microcontrollers, digital signal processors, less-general AIP environments, selecting microprocessors, general purpose processor design.

UNIT 2. **(05Hrs)**

ARCHITECTURE OF ARM7TDMI processor, Programming model, Registers, Operating modes, Instruction set, Addressing modes, memory interface.

UNIT 3. **(05Hrs)**

PERIPHERALS: Introduction, timers, counters and watchdog timers, UART, Pulse width modulators, controlling a DC motor using PWM, LCD controllers, Keypad controllers, stepper motor controllers, ADCs, Real time clocks.

UNIT 4. **(06Hrs)**

MEMORY: Memory write ability and storage permanence, common memory types, composing memory, memory hierarchy and cache, advanced RAM.

UNIT 5. **(07Hrs)**

INTERFACING: Introduction, Communication basics, Basic protocol concepts, ISA bus protocol: memory access, Arbitration, Priority arbiter, Daisy chain Arbitration, wireless communication, Layering, error detection and correction, wireless protocols: IrDA, Bluetooth, IEEE802.11

UNIT 6. **(05Hrs)**

INTRODUCTION TO ARM 9, ARM926EJ-S, Features, Specifications (LPC314x /LPC315x as reference controllers)

REFERENCE BOOKS:

1. Rajkamal,'Embedded System – Architecture Programming and Design',Tata-McGraw Hill Pub.
2. Dr.K.V.K.K.Prasad 'Embedded Real Time Systems' Dreamtech
3. Andrew Sloss Embedded System Developers'
4. Frank Vahid and Tony Givargis, Embedded system design: A unified hardware/software introduction, John Wiley and Sons, 2002
5. Data Sheet of ARM7TDMI
6. Data Sheet of ARM926EJ-S , (LPC314x /LPC315x)

SEMESTER-II

MEX654 – REAL TIME OPERATING SYSTEM

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08 Hrs)**

REAL TIME SYSTEMS CONCEPTS: real time systems concepts such as foreground/background systems, critical sections, resources, multitasking, context switching, scheduling, reentrancy, task priorities, mutual exclusion, semaphores, intertask communications, interrupts and more.

UNIT 2. **(08Hrs)**

KERNEL STRUCTURE : Introduction to μC/OS-II and its internal structure. Tasks, task states, task control blocks, how μC/OS-II implements a ready list, task scheduling, the idle task, Determination of CPU usage, μC/OS-II handles interrupts, Initialization and start μC/OS-II and more.

UNIT 3. **(04 Hrs)**

TASK MANAGEMENT: μC/OS-II's service to crate a task, delete a task, check the size of a task's stack, change a task's priority, suspend and resume a task, and get information about a task.
TIME MANAGEMENT: μC/OS-II Time management Services

UNIT 4. **(08Hrs)**

INTERTASK COMMUNIATION AND SYNCHRONIZATION: μC/OS-II's services to have tasks and ISRs (Interrupt Service Routines) communicate with one another and share resources.
Semaphores, massage mailboxes, and massage queues Implementation.

UNIT 5. **(04Hrs)**

MEMORY MANAGENT: μC/OS-II's dynamic memory allocation feature using fixed –sized memory blocks.

UNIT 6. **(08Hrs)**

Porting µC/OS-II: Porting of µC/OS-II to ARM_7TDMI processor architectures. Application development using µC/OS-II and ARM Processor.

REFERENCE BOOKS:

1. Jean Lambrosse : Micro COS-II: The Real –Time Kernel
2. Jean Lambrosse, Embedded system building Blocks, R&D Books, Lawrence
3. Rajkamal, Embedded System, Tata –Mc Grew Hill Publications
4. Phillips, LPC-ARM Processor Application Notes

MES691 – ADVANCE COMPUTER ARCHETECHER (EL-II)

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08 Hrs)**

INTRODUCTION TO SUBJECT: Principles of scalable performance:-Performance metrics and measures, parallel processing applications, scalability analysis and approaches.
Bus, cache and shared memory:-Back plane bus systems, Cache memory organization and shared memory organizations. Flynn's classifications.

UNIT 2. **(07 Hrs)**

PIPELINING TECHNIQUES:- Linear pipeline processors, nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design.

UNIT 3. **(07 Hrs)**

SUPER SCALAR TECHNIQUES: Super scalar and super-pipeline design
SIMD array processors: - features and organization, interconnecting networks, parallel algorithms for array processors,

UNIT 4. **(06 Hrs)**

ASSOCIATIVE ARRAY PROCESSING AND PROCESSORS: Performance enhancement of array processors. Vector processing principles and vector instructions, Vector processors

UNIT5. **(06 Hrs)**

MULTIPROCESSOR AND MULTICOMPUTER:-Structures, multiprocessor system interconnects, cache coherence and synchronization mechanisms, Three generations of multi-computers , message passing mechanisms.

UNIT 6. **(06 Hrs)**

RISC PROCESSORS: The VLIW Architecture, case studies of at least two of the architectures studied above.

Brief introduction to parallel processing models and languages

REFERENCE BOOKS:

1. Advanced Computer Architecture by Kai Wang ,TMH.
2. Computer Architecture and parallel preprocessing, by Kai Wang and F.A.Briggs. Mc Graw Hill (IE)
3. Computer Organization and Architecture by W. Stalling, MC Millan.
4. High Performance Computer Architecture H.S.Store, Addition Wesley.
5. Modern processor Design: Fundamentals of Super scalar Processors She
6. Computer Architecture And Organization An Integrated Approach By Miles Murdocca And Vincent Heuring
7. Computer System Architecture And Organization By Dr. M.Usha And T.S. Shrikanth

MES692 – STATISTICAL SIGNAL PROCESSING (EL-II)

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08Hrs)**

REVIEW OF RANDOM VARIABLES:
Distribution and density functions, moments, independent, uncorrelated and orthogonal random variables; Vector-space representation of Random variables, Schwarz Inequality Orthogonalit principle in estimation, Central Limit theorem, Random processes, wide-sense stationary processes, autocorrelation and auto covariance functions, Spectral representation of random signals, Wiener Khinchin theorem Properties of power spectral density, Gaussian Process and White noise process, Linear System with random input, Spectral factorization theorem and its importance, innovation process and whitening filter, .Random signal modeling: MA(q), AR(p) , ARMA(p,q)models.

UNIT 2. **(08Hrs)**

PARAMETER ESTIMATION THEORY:
Principle of estimation and applications, Properties of estimates, unbiased and consistent estimators, Minimum Variance Unbiased Estimates (MVUE), Cramer Rao bound, Efficient estimators; Criteria of estimation: the methods of maximum likelihood and its properties ; Baysean estimation : Mean square error and MMSE, Mean Absolute error, Hit and Miss cost function and MAP estimation.

UNIT 3. **(06Hrs)**

ESTIMATION OF SIGNAL IN PRESENCE OF WHITE GAUSSIAN NOISE:
Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hoff Equation, FIR Wiener filter, Causal IIR Wiener filter, Noncausal IIR Wiener filter, Linear

UNIT 4. **(06Hrs)**

ADAPTIVE FILTERING:
Principle and Application, Steepest Descent Algorithm Convergence characteristics; LMS algorithm, convergence, excess mean square error, Leaky LMS algorithm; Application of Adaptive filters ;RLS algorithm, derivation, Matrix inversion Lemma, Initialization, tracking of nonstationarity.

UNIT 5. **(04Hrs)**

KALMAN FILTERING:
State-space model and the optimal state estimation problem, discrete Kalman filter, continuous-time Kalman filter, extended Kalman filter.

UNIT 6. **(08Hrs)**

SPECTRAL ANALYSIS: Estimated autocorrelation function, periodogram, Averaging the periodogram (Bartlett Method), Welch modification, Blackman and Tukey method of smoothing periodogram, Prametric method, AR(p) spectral estimation and detection of Harmonic signals, MUSIC algorithm.

REFERENCE BOOKS:

1. M. Hays: Statistical Digital Signal Processing and Modelling, John Willey and Sons, 1996.
2. M.D. Srinath, P.K. Rajasekaran and R. Viswanathan: Statistical Signal Processing with Applications, PHI, 1996.
3. Simon Haykin: Adaptive Filter Theory, Prentice Hall, 1996.
4. D.G. Manolakis, V.K. Ingle and S.M. Kogon: Statistical and Adaptive Signal Processing, McGraw Hill, 2000.
5. S. M. Kay: Modern Spectral Estimation, Prentice Hall, 1987.

MES693 – RECONFIGURABLE COMPUTING (EL-II)

Teaching Scheme:
Lecture - 03 Hrs
Tutorial - 01 Hrs

Examination Scheme:
Theory Paper - 80 Marks
Class Test - 20 Marks
Credit:-04

UNIT 1. **(08 Hrs)**

INTRODUCTION TO RECONFIGURABLE COMPUTING

Introduction to Reconfigurable Computing, Basic concepts and related fields of study, Performance, power, and other metrics - Algorithm analysis and speedup projections, RC Architectures, Device characteristics, Fine-grained architectures, Coarse grained architectures.

UNIT 2. **(08 Hrs)**

FPGA DESIGN

Introduction to FPGA, FPGA Physical Design Tools, Technology mapping, Placement & Partitioning Algorithms, Routing Algorithms, Register transfer (RT)/Logic Synthesis, Controller/Data path synthesis, Logic minimization.

UNIT 3. **(04 Hrs)**

PARALLEL PROCESSING

RC Application, Design, Parallelism, Systolic arrays, Pipelining, Optimizations, Bottlenecks, High-level Design - High-level synthesis - High-level languages - Design tools, Debugging.

UNIT 4. **(08 Hrs)**

RECONFIGURABLE SYSTEMS

Adaptive Network Architectures, Static and Dynamic network, Routing/embedding Rearrangeable networks, Reconfigurable bus, Dynamic reconfiguration issues, Reconfiguration delay, OS support, Reconfigurable Operating Systems, Device and task models, Multitasking and runtime systems.

UNIT 5. **(08 Hrs)**

RECONFIGURABLE PROCESSORS

Reconfigurable Computing Architectures, Reconfigurable coprocessor based architectures, Compiler technology for coprocessor based architectures, Mapping/scheduling algorithm, Reconfigurable pipelines, Reconfigurable memories & caches.

UNIT 6. **(04 Hrs)**

CASE STUDY

Case Studies- Signal Processing, Image & Video processing, Bioinformatics, Cryptography, Security - Special Topics – Dynamic & Partial Reconfiguration - Numerical Analysis - Performance Analysis/Prediction - Fault Tolerance

REFERENCE BOOKS:

1. C. Maxfield, "The Design Warrior's Guide to FPGAs: Devices, Tools and flows", Newnes, 2004.
2. M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
3. C. Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer, 2007.
4. John V.Oldfield and Richard C. Dorf, "Field Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems", John Wiley & Sons, Inc., 1995.
5. Configware Reiner W. Hartenstein, Viktor K. Prasanna (Eds.): "Reconfigurable Architectures: High Performance", IT press Verlag, 1997.
6. Wayne Wolf, "FPGA- based System Design", Prentice Hall, 2004..

SEMESTER-II

MES672 – EMBEDDED LAB-II

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Practical Hours:-04 H/Week	Term work:-50 Marks
	Credit:-02

Students are instructed to frame and perform laboratory assignment based on each of theory course. The assignment should encompass the hardware and software techniques/tools introduced in the concerned subjects and should prove to be useful for the PG program in the relevant field. Assignment should be a full-fledged system design problems with multidimensional solutions suggested.

Student shall submit a laboratory work document based on the assignment performed at the end of semester. The laboratory instructor shall guide the students in framing the assignments and defining the problems pertaining to the said subjects.

SEMESTER-II

MES672 – SYSTEM LAB-II

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial -NA	Class Test - NA
Practical Hours-02 H/Week	Practical- 50 Marks
	Credit-01

Individual student will perform the work as per the following guidelines and submit the report based on result obtained and /or study performed under the guidance of respective guide (Minimum 25 pages).

The work will be assessed by two examiners out of which one will be external examiner appointed by the University and second examiner (internal) will be guide itself.

Work to be carried out by student,

1) Student should perform experimentation in any subject of the stream as assign by the respective guide, leading towards concept understanding.
2) Literature survey about the topic, research and development or thrust area subject.
3) Student should build any one of the software/Hardware based mini project as per guidelines given by respective committee and/or guide.

SEMESTER-II

MES673 – SEMINAR-II

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Hours:-02 H/Week	Seminar:-50 Marks
	Credit:-01

Student should deliver seminar on the state of the art topic infront of the external examiners and internal examiners, staff and student colleagues. Prior to presentation student should carry the details of literature survey form standard references such as international journals and periodicals, recently published reference books etc. student should submit a report on same along with computer based presentation copy to the concerned examiner/guide at the end of seminar. The assessment shall be based on selection of topic its relevance to present context, report documentation and presentation skills.

SEMESTER-III

MES731 – DISSERTATION-I

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Hours:-12 H/Week	Term work:-50 Marks
	Practical Oral-50 marks
	Credit:-12

The dissertation Seminar will consist of a type written report covering the topic selected for Final Dissertation. This should include the literature survey, technical details and related data required for the proposed dissertation work. The candidate shall deliver the dissertation seminar on the topic which will be judged by two examiners (one external and one internal guide). The assessment shall be based on selection of topic its relevance to present context, report documentation and presentation skills, utility of the dissertation work & publications based on the same.

SEMESTER-IV

MES781 – DISSERTATION-II

Teaching Scheme:	Examination Scheme:
Lecture - NA	Theory Paper - NA
Tutorial - NA	Class Test - NA
Hours:-20 H/Week	Term work:-100 Marks
	Practical Oral-200 marks
	Credit:-20

The student shall be allowed to submit the dissertation- II report only after the completion of dissertation- I. Student should deliver Viva-Voca Presentation on topic of Desertaion-II infront of the external examiners and internal examiners, staff and student colleagues The assessment shall be based on design and implementation aspects, report documentation and presentation skills, utility of the dissertation work & publications based on the same.